OIPE JC179
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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application for:

Steven Teig et al

Serial No.: 09/681,776

Filing Date: 6/3/2001

For: DIAGONAL WIRING ARCHITECTURE FOR INTEGRATED CIRCUITS

Examiner: Nguyen, Dao H.

Group Art Unit: 2818

APPEAL BRIEF

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal from the final rejection of claims 1-3, 5-13, and 15-20 in the above-referenced application. In accordance with 37 C.F.R. §1.192, this Brief, along with the accompanying Appendix, is filed in triplicate and is accompanied by the required fee. Please charge any additional fees or credit any overpayment to Deposit Account No. 50 1128.

I. REAL PARTY IN INTEREST

The real party in interest to this Appeal is Cadence Design Systems, a Delaware Corporation, having its principal place of business in San Jose, California.

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II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellants, the Appellants' legal representative, or assignees thereof.

III. STATUS OF CLAIMS

On September 3, 2003, Appellants appealed from the final rejection of claims 1-3, 5-13, and 15-20. Claims 4 and 14 were cancelled in response to the Examiner's duplicate claims objection. Some of claims 21-47 were cancelled in response to the Examiner's restriction requirement. The remainder of claims 21-47 were cancelled by Appellants in a Preliminary Amendment.

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Concurrent with the Notice of Appeal, Appellants filed an Amendment making a minor correction to claim 1 in response to a 35 U.S.C. §112, second paragraph rejection which was asserted by the Examiner in the Final Office Action mailed April 3, 2003. To date, the Appellants have not received an Advisory Action from the Examiner indicating whether this amendment was entered.

The Appellants are filing an Amendment concurrent with this Appeal to clarify the subject matter recited in claims 1 and 11. For the reasons explained in the Remarks section of that Amendment, Appellants believe those claim amendments are entitled to entry under the standards set forth in MPEP §714.12 and MPEP §1207.

V. SUMMARY OF INVENTION

Appellants' invention comprises both an integrated circuit having wires deposed in a diagonal direction and a method for simulating a wiring direction (for example, on an integrated circuit) using either wires deposed in diagonal directions, wires deposed in Manhattan directions, or a combination of wires deposed in diagonal and Manhattan directions. The Examiner imposed a restriction requirement that included the integrated circuit claims in one group and the method claims in the other group. Appellants elected the former group without traverse. A portion of the former group is on appeal. These elected claims are set forth in the Appendix to this brief.

In one embodiment of Appellants' invention, an integrated circuit comprises at least one metal layer. The metal layer includes conductors which interconnect components on the integrated circuit . For purposes of assigning preferred wiring directions for the conductors, the metal layer is divided into at least two sections (e.g., first section and second section). *Specification, paragraph 0003.* Each section contains at least one thousand wires (*i.e.*, conductors) to interconnect points on the integrated circuit. *Specification, paragraph 0003.* The conductors in each section are oriented in a preferred direction relative to the boundaries of the integrated circuit. A "preferred direction" is a direction in which at least fifty percent of the conductors are oriented. *Specification, paragraph 0003.* **Figure 10** illustrates an example metal layer with multiple preferred directions.

The first and second sections of the claimed integrated circuit have different preferred wiring directions. One of the sections has a preferred wiring direction that is diagonal. A diagonal direction

is neither vertical nor horizontal. Examples of diagonal directions include octalinear (*i.e.*, plus or minus 45 degrees from vertical or horizontal) and hexalinear (*i.e.*, plus or minus 30 or 60 degrees from vertical or horizontal). *Specification, paragraph 0034.* **Figure 1b** illustrates an example of an integrated circuit that employs diagonal wiring. Furthermore, one of the sections contains at least one conductor deposed in a Manhattan direction coupled to a conductor deposed in a diagonal wiring direction. *See, for example,* ***Figure 14.*** A "Manhattan direction" is either vertical or horizontal. *Specification, paragraph 0034.* **Figure 6a** illustrates an embodiment for a legacy Manhattan metal layer configuration.

VI. ISSUES

Claims 1-3 and 5-10 were rejected under 35 U.S.C. §112, second paragraph as indefinite. Claims 1-3 and 5-10 were rejected under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 6,316,838 to Kaname Ozawa et al (hereinafter referred to as "Ozawa") in view of remarks made by the Examiner. Claims 11-13 and 15-20 were rejected under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 5,822,214 to Michael D. Rostoker et al (hereinafter referred to as "Rostoker") in view of remarks made by the Examiner or in view of Ozawa.

VII. GROUPING OF THE CLAIMS

Appellants are grouping the claims. Group 1 comprises claims 1-3 and 5-10. Group 2 comprises claims 11-13 and 15-20.

VIII. THE EXAMINER'S RATIONALE

The Examiner's rationale for rejecting claims 1-3 and 5-10 under the second paragraph of 35 U.S.C. §112 is stated as follows in his Final Rejection: the phrase "said conductors" in claim 1, line 7 was not clearly defined. The Examiner asserts that it is not clear whether "said conductors" includes all conductors in the first and the second region or just includes the conductors in the second region. He queries whether there was any difference between "said conductors" in line 5 of claim 1 and "said conductors" in line 7 of claim 1. He also states that because claims 2, 3, and 5-10 depend from rejected claim 1 and include all of the limitations of claim 1, these dependent claims are also indefinite.

The Examiner's rationale for rejecting claims 1-3 and 5-10 as obvious in view of Ozawa and his remarks is stated as follows in his Final Rejection: Ozawa describes (in Figures 4 and 5) all the elements of claim 1 except that Ozawa does not specifically teach that the first contiguous region comprises an area of at least 100 square microns. The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made that the region of Ozawa could be modified to have any area either greater, less than, or equal to 100 square microns since such a modification would have involved a mere change in the size of a component. Citing In re Rose, 105 USPQ 237 (CCPA 1955); he also asserts that a change in size is generally recognized as being within the ordinary skill in the art. Regarding claims 2, 3, and 5-10; the Examiner admits that Ozawa does not specifically describe the angle created by the diagonal direction

conductor relative to the boundaries of the integrated circuit. However, he asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made that the diagonal conductors of Ozawa could be made in any angle relative to the boundaries of the integrated circuit.

The Examiner's rationale for rejecting claims 11-13 and 15-20 as obvious in view of Rostoker and his remarks or in view of Ozawa was stated as follows, also in his Final Rejection: Rostoker describes (in Figures 2-10) all the elements of claim 1 except that Rostoker does not specifically discuss a zag conductor. However (because Rostoker states that tri-direction, hexagonal routing, and rectilinear routing may be used to connect the terminals and the gates of the device (See Rostoker at Col. 6, lines 7-15, Col. 7, lines 1-20, and Col. 7, line 60-Col. 8, line 4)) it would have been obvious to one having ordinary skill in the art at the time the invention was made that Rostoker does have zag conductors which connect the contacts from the outside to the diagonal lines. The Examiner asserts that, on the other hand, Ozawa discloses a metal layer having diagonal conductors 62 and zag conductors connecting the vias 60 to the pad 58. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Rostoker so that the zag conductors described in Ozawa connect separated equi-electrodes together (See Col. 6, lines 45-49 of Ozawa). The Examiner goes on to assert that Figures 2-4 of Rostoker disclose all the limitations of claims 12, 13, and 15-18. Next, regarding claims 19 and 20, the Examiner admits that Rostoker does

not specifically describe the direction of the zag conductors. However, the Examiner asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made that the direction of the zag could be made either horizontal or vertical since none of those directions would make a difference in the scope of Rostoker. In addition, the Examiner says that such various directions could be made involving only routine skill in the art.

Finally, the Examiner asserts that Rostoker in view of Ozawa disclose all the claimed limitations for reasons similar to the reasons he described above with respect to his rejection of claims 9 and 10.

IX. ARGUMENT

A. The Section 112, Second Paragraph Rejection of Claims 1-3 and 5-10

Concurrent with the Notice of Appeal in this case, Appellants filed an amendment to claim 1 to address the Examiner's indefiniteness rejection. Appellants respectfully submit that the amendment to claim 1 presented with the Notice of Appeal (and repeated in the amendment attached to this Appeal Brief) properly addresses the Examiner's concerns. Accordingly, Appellants respectfully request withdrawal of the 35 U.S.C. §112 rejection of claims 1-3 and 5-10.

B. The Section 103 Rejections of Claims 1-3 and 5-10

Appellants respectfully submit that Ozawa in view of the Examiner's remarks does not render claims 1-3 and 5-10 obvious for at least the following reasons.

1. The *Prima Facie* Case of Obviousness

The legal concept of *prima facie* obviousness is a procedural tool of examination which applies broadly to all arts. A prima facie case of obviousness is one that will stand unless rebutted by evidence. It is the burden of the examiner to establish a prima facie case of obviousness when rejecting claims under 35 U.S.C. §103. In re Piasecki, 754 F.2D 1468, 223 USPQ 758 (Fed. Cir. 1985); MPEP §2142.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Next, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000).

2. The combination of Ozawa and the Examiner's Remarks does not teach all the elements recited in claims 1-3 and 5-10

Appellants respectfully submit that Ozawa in view of the Examiner's remarks does not teach all the elements of claim 1 because neither Ozawa nor the Examiner's

remarks teach either the element of "at least one metal layer" or the element of "at least one zag conductor . . . so as to interconnect components on said integrated circuit" as recited in amended claim 1. In one embodiment, Ozawa describes a semiconductor device comprising a substrate and two semiconductor elements each attached to different surfaces of the substrate. The substrate further comprises built in wires which enable the electrodes of one semiconductor element to be connected to electrodes of the other semiconductor element. Col. 2, lines 21-43. The semiconductor device described in Ozawa is intended to solve problems associated with connecting electrodes between two semiconductor elements when the electrode layouts of the semiconductor elements are different (i.e., the electrodes of one semiconductor element and the electrodes of the other semiconductor element (when the semiconductor elements are attached to opposite surfaces of the substrate) cannot be connected through an imaginary line perpendicular to the surface of the substrate). Prior to Ozawa, large loops of wires would be required to connect the electrodes of semiconductor elements attached to a substrate when the electrode layouts for the semiconductor elements were different. Col. 6, lines 50-64.

In the Final Office Action, the Examiner suggests that the substrate 33 described in Ozawa teaches the at least one metal layer element recited in claim 1. However, nothing in Ozawa describes the substrate 33 as being comprised of metal. In fact, Ozawa states that the substrate may be made of "polyimide" or "glass epoxy" as the basic

material. Col. 5, lines 38-42. Thus, Ozawa does not teach a metal layer as recited in amended claim 1.

In addition to failing to teach the "at least one metal layer" element of claim 1, nothing in Ozawa teaches utilizing a zag conductor to interconnect components of an integrated circuit as recited in amended claim 1. As mentioned above, Ozawa teaches a method for interconnecting electrodes of semiconductor devices. As defined in Appellants' specification, components of an integrated circuit may include electronic components (such as transistors, resistors, and diodes) and circuit components (such as gates, cells, arithmetic units, controllers, and decoders). Nothing in Ozawa teaches interconnecting components as recited in amended claim 1.

In addition to failing to teach both the "at least one metal layer" element and the interconnection of components element, Ozawa also fails to teach the element of amended claim 1 which recites that the first contiguous region comprises an area of at least 100 square microns. The Examiner admits to this deficiency in the Final Office Action. To make up for this Ozawa deficiency, the Examiner cites In re Rose, 105 USPQ 237 (CCPA 1955), and asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify what he asserts is a first contiguous region of Ozawa to have any area greater than, less than, or equal to 100 square microns. MPEP §2144 states that if the facts in a prior legal decision are sufficiently similar to those in an application under examination, the examiner may use the rationale used by the

court. However, the facts of In re Rose are not at all similar to the present application. In In re Rose, the claims were directed to a lumber package. The claim language recited that the weight of lumber packages covered by the scope of that claim were lumber packages "of appreciable size and weight requiring handling by a lift truck". Id. The court held this claim to be unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art. Id. In addition to the fact that the subject matter of In re Rose (a lumber package) is nonanalogous to the art area of the present application (conductors within integrated circuits), the claim language was very vague: of appreciable size and weight requiring handling by a lift truck. In the present case, the claim language in question is very specific: an area of a metal layer of at least 100 square microns. Thus, Appellants respectfully submit that the facts of In re Rose are not sufficiently similar to the facts of the present application as required by MPEP §2144 and that In re Rose has not been properly cited by the Examiner to support the 35 U.S.C. §103 rejection of claims 1-3 and 5-10.

In addition to respectfully submitting that the Examiner has improperly cited In re Rose to make up for the deficiency that Ozawa does not teach the 100 square micron element of claim 1, Appellants respectfully disagree with the Examiner's assertion that this same deficiency of Ozawa may be made up because a change in size in the context of the 100 square micron element recited in claim 1 would be well known to one of ordinary

skill in the art at the time the present invention was made. Thus, in accordance with MPEP §2144.03, the Examiner is requested to provide a reference or references supporting all of the features the Examiner believes are "well known". If the rejection is based on facts within the personal knowledge of the Examiner, the Examiner is requested to support the rejection with an affidavit setting forth the facts upon which the Examiner's rejection is based. See 37 C.F.R. 1.104(d)(2). Appellants should be given an opportunity to address the new reference(s) or affidavit.

In view of the above, Appellants respectfully submit that the Ozawa in view of the Examiner's remarks does not render obvious the subject matter of claim 1 because this combination does not teach each element of claim 1. Withdrawal of this rejection of claim 1 under 35 U.S.C. §103(a) is, therefore, requested.

As for claims 2, 3, and 5-10, each of these claims is dependent either directly or indirectly from independent claim 1. Accordingly, the arguments made above apply equally to these claims. Withdrawal of the rejection of claims 2, 3, and 5-10 under 35 U.S.C. §103 is therefore requested.

C. The Section 103 Rejections of Claims 11-13 and 15-20

Appellants respectfully submit that Rostoker in view of the Examiner's remarks or in view of Ozawa does not render claims 11-13 and 15-20 obvious for at least the following reasons.

Appellants respectfully submit that Rostoker in view of the Examiner's remarks or in view of Ozawa does not teach all the elements of claim 11 because neither Rostoker, the Examiner's remarks, nor Ozawa teach "at least one zag conductor coupled to a conductor deposed in a first diagonal direction, . . . said zag conductor being on a same metal layer as said conductor deposed in the first diagonal direction." as recited in claim 11. Rostoker teaches an architecture which provides electrical conductors for interconnection. Col. 6, lines 31-33. In accordance with the preferred embodiment, three separate metal layers comprise conductors. The conductors on each metal layer extend in three different directions that are angularly displaced from each other by 60 degrees. Thus, for example, the conductors of metal layer 1 are displaced 60 degrees in direction from the conductors of metal layer 2; the conductors of metal layer 2 are displaced 60 degrees in direction from the conductors of metal layer 3. Col. 6, lines 31-48. Deposing the conductors as described above provides more than the traditional two directions of interconnect routing provided by the prior art. Col. 4, lines 54-60. According to Rostoker, this architecture is advantageous because these additional routing directions reduce the total wirelength interconnect congestion of integrated circuits. Col. 6, lines 48-54. However, unlike the present invention, nothing in Rostoker teaches coupling conductors to each other wherein the coupled conductors are on the same metal layer. In fact, unlike the present invention as recited in claim 1, Rostoker teaches away from

coupling conductors on the same metal layer wherein the conductors are deposed in different directions:

> Conductors that extend in the three directions can be formed in three different layers, or alternatively the conductors that extend in two or three of the directions can be formed in a single layer as long as they do not cross. Col. 7, lines 60-63.

See also Rostoker at Col. 17, lines 1-6. Unlike the coupling recited in claim 11, Rostoker teaches that the conductors within a same metal layer should not cross. When the prior art teaches away from the present invention, a per se demonstration that there is a lack of prima facie obviousness arises. In re Dow Chemical Co., 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1988).

In addition to failing to teach coupling of conductors within a single metal layer as recited in claim 11, the Examiner admits that Rostoker does not explicitly teach zag conductors. The Examiner suggests that Rostoker implicitly teaches zag conductors at Col. 6, lines 7-15, Col. 6, lines 1-20, and Col. 7, line 60-Col. 8, line 4. Appellants respectfully submit that these sections of Rostoker do not teach a zag conductor coupled to a conductor deposed in a diagonal direction as recited in claim 11. Appellants respectfully disagree with the Examiner's conclusion that it would have been obvious to one of ordinary skill in the art at the time the invention was made that Rostoker teaches zag conductors coupled to conductors deposed in a diagonal direction. Thus, in accordance with MPEP §2144.03, the Examiner is requested to provide a reference or

references supporting all of the features the Examiner believes are "well known". If the rejection is based on facts within the personal knowledge of the Examiner, the Examiner is requested to support the rejection with an affidavit setting forth the facts upon which the Examiner's rejection is based. See 37 C.F.R. 1.104(d)(2). Appellants should be given an opportunity to address the new reference(s) or affidavit.

Appellants respectfully submit that there is no motivation to combine the teachings of Rostoker and Ozawa. The mere fact that references can be combined or modified does not render the resultant combination obvious, unless the prior art also suggests the desirability of the combination. In re Kotzab, supra. It is improper to use the inventor's disclosure as a road map for selecting and combining prior art disclosures. Grain Processing Corp. v. American Maize-Products Corp., 840 F.2d 902, 907 (Fed. Cir. 1988). Absent such a showing in the prior art, the Examiner has impermissibly used "hindsight" by using the Appellants' teaching as a blueprint to hunt through the prior art for the claimed elements and combine them as claimed. In re Zuko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997). Appellants respectfully submit that the Examiner is relying on an improper hindsight reconstruction, which cannot be used for rejecting the claims of the above-identified application. Nothing in Rostoker or Ozawa teach or suggest combining the teachings of their respective disclosures.

Because Rostoker does not teach coupling a zag conductor to a conductor deposed in a diagonal direction wherein both conductors are on the same metal layer, because the Examiner admits that Rostoker fails to teach the zag conductor element, and because there is no motivation to combine Rostoker and Ozawa, the combination of Rostoker in view of the Examiner's remarks or in view of Ozawa does not render claim11 obvious under 35 U.S.C. §103(a). Accordingly, Appellants respectfully request withdrawal of the rejection of claim 11.

As for claims 12, 13, and 15-20, each of these claims is dependent either directly or indirectly from independent claim 11. Accordingly, the arguments made above apply equally to these claims. Withdrawal of the rejection of claims 12, 13, and 15-20 under 35 U.S.C. §103 is therefore requested.

X. CONCLUSION.

For the foregoing reasons, Appellants believe that the Examiner's rejections of claims 1-3, 5-13, and 15-20 were erroneous, and reversal of his decisions is respectfully requested.

BY: Earl D. Brown Jr.

Earl D. Brown, Jr.
Reg. No. 44,042
Date: January 8, 2004
Tel. No.: 650.752.0990 ext. 103

APPENDIX

The following claims are the subject of this Appeal.

1. An integrated circuit comprising:

at least one metal layer comprising a plurality of regions, wherein a first contiguous region comprises an area of said metal layer of at least 100 square microns and comprises a plurality of conductors to interconnect components on said integrated circuit, said conductors comprising a plurality of preferred diagonal direction conductors and at least one zag conductor, and wherein a second contiguous region comprises a plurality of conductors such that at least fifty (50) percent of said conductors of the second contiguous region are arranged in a preferred direction other than said preferred diagonal direction;

said preferred diagonal direction conductors comprising at least fifty (50) percent of said conductors in said first region and being deposed in a preferred diagonal direction that forms a Euclidean angle relative to the boundaries of the integrated circuit, and

said at least one zag conductor being deposed in a Manhattan direction and being coupled to one of said preferred diagonal direction conductors so as to interconnect components on said integrated circuit using at least one zag conductor and at least one preferred diagonal direction conductor.

2. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises plus 45 degrees relative to the boundaries of said integrated circuit.

3. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises minus 45 degrees relative to the boundaries of said integrated circuit.

Claim 4 (cancelled)

5. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises plus 60 degrees relative to the boundaries of said integrated circuit.

6. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises minus 60 degrees relative to the boundaries of said integrated circuit.

7. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises plus 30 degrees relative to the boundaries of said integrated circuit.

8. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises minus 30 degrees relative to the boundaries of said integrated circuit.

9. The integrated circuit of claim 1, wherein said Manhattan direction of said at least one zag comprises a horizontal direction relative to the boundaries of said integrated circuit.

10. The integrated circuit of claim 1, wherein said Manhattan direction of said at least one zag comprises a vertical direction relative to the boundaries of said integrated circuit.

11. An integrated circuit comprising:

a plurality of metal layers with each metal layer comprising a plurality of conductors to interconnect components on the integrated circuit, at least fifty (50) percent of said conductors on a first metal layer being deposed in a first preferred diagonal direction, wherein said first preferred diagonal direction defines a direction that forms a Euclidean angle relative to the boundaries of the integrated circuit, for at least fifty percent of conductors on said first metal layer;

at least fifty (50) percent of said conductors on a second metal layer arranged in a second preferred diagonal direction, wherein said second preferred diagonal direction defines a direction, different than said first preferred diagonal direction, that forms a Euclidean angle relative to the boundaries of the integrated circuit; and

at least one zag conductor, coupled to a conductor deposed in a first diagonal direction, said zag conductor being deposed in a Manhattan direction so as to interconnect components on said integrated circuit using at least one zag conductor and at least one conductor arranged in said first preferred diagonal direction, said zag conductor being on a same metal layer as said conductor deposed in the first diagonal direction.

12. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises plus 45 degrees and said second preferred diagonal direction comprises minus 45 degrees relative to the boundaries of said integrated circuit.

13. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises minus 45 degrees and said second preferred diagonal direction comprises plus 45 degrees relative to the boundaries of said integrated circuit.

Claim 14 (cancelled)

15. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises plus 60 degrees and said second preferred diagonal direction comprises minus 60 degrees relative to the boundaries of said integrated circuit.

16. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises minus 60 degrees and said second preferred diagonal direction comprises plus 60 degrees relative to the boundaries of said integrated circuit.

17. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises plus 30 degrees and said second preferred diagonal direction comprises minus 30 degrees relative to the boundaries of said integrated circuit.

18. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises minus 30 degrees and said second preferred diagonal direction comprises plus 30 degrees relative to the boundaries of said integrated circuit.

19. The integrated circuit of claim 11, wherein said Manhattan direction of said at least one zag conductor comprises a horizontal direction relative to the boundaries of said integrated circuit.

20. The integrated circuit of claim 11, wherein said Manhattan direction of said at least one zag conductor comprises a vertical direction relative to the boundaries of said integrated circuit.

Claims 21-47 (cancelled)

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The real party in interest to this Appeal is Cadence Design Systems, a Delaware Corporation, having its principal place of business in San Jose, California.

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The first and second sections of the claimed integrated circuit have different preferred wiring directions. One of the sections has a preferred wiring direction that is diagonal. A diagonal direction

is neither vertical nor horizontal. Examples of diagonal directions include octalinear (*i.e.*, plus or minus 45 degrees from vertical or horizontal) and hexalinear (*i.e.*, plus or minus 30 or 60 degrees from vertical or horizontal). *Specification, paragraph 0034.* **Figure 1b** illustrates an example of an integrated circuit that employs diagonal wiring. Furthermore, one of the sections contains at least one conductor deposed in a Manhattan direction coupled to a conductor deposed in a diagonal wiring direction. *See, for example,* ***Figure 14***. A "Manhattan direction" is either vertical or horizontal. *Specification, paragraph 0034.* **Figure 6a** illustrates an embodiment for a legacy Manhattan metal layer configuration.

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The Examiner's rationale for rejecting claims 1-3 and 5-10 as obvious in view of Ozawa and his remarks is stated as follows in his Final Rejection: Ozawa describes (in Figures 4 and 5) all the elements of claim 1 except that Ozawa does not specifically teach that the first contiguous region comprises an area of at least 100 square microns. The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made that the region of Ozawa could be modified to have any area either greater, less than, or equal to 100 square microns since such a modification would have involved a mere change in the size of a component. Citing In re Rose, 105 USPQ 237 (CCPA 1955); he also asserts that a change in size is generally recognized as being within the ordinary skill in the art. Regarding claims 2, 3, and 5-10; the Examiner admits that Ozawa does not specifically describe the angle created by the diagonal direction

conductor relative to the boundaries of the integrated circuit. However, he asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made that the diagonal conductors of Ozawa could be made in any angle relative to the boundaries of the integrated circuit.

The Examiner's rationale for rejecting claims 11-13 and 15-20 as obvious in view of Rostoker and his remarks or in view of Ozawa was stated as follows, also in his Final Rejection: Rostoker describes (in Figures 2-10) all the elements of claim 1 except that Rostoker does not specifically discuss a zag conductor. However (because Rostoker states that tri-direction, hexagonal routing, and rectilinear routing may be used to connect the terminals and the gates of the device (See Rostoker at Col. 6, lines 7-15, Col. 7, lines 1-20, and Col. 7, line 60-Col. 8, line 4)) it would have been obvious to one having ordinary skill in the art at the time the invention was made that Rostoker does have zag conductors which connect the contacts from the outside to the diagonal lines. The Examiner asserts that, on the other hand, Ozawa discloses a metal layer having diagonal conductors 62 and zag conductors connecting the vias 60 to the pad 58. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Rostoker so that the zag conductors described in Ozawa connect separated equi-electrodes together (See Col. 6, lines 45-49 of Ozawa). The Examiner goes on to assert that Figures 2-4 of Rostoker disclose all the limitations of claims 12, 13, and 15-18. Next, regarding claims 19 and 20, the Examiner admits that Rostoker does

not specifically describe the direction of the zag conductors. However, the Examiner asserts that it would have been obvious to one having ordinary skill in the art at the time the invention was made that the direction of the zag could be made either horizontal or vertical since none of those directions would make a difference in the scope of Rostoker. In addition, the Examiner says that such various directions could be made involving only routine skill in the art.

Finally, the Examiner asserts that Rostoker in view of Ozawa disclose all the claimed limitations for reasons similar to the reasons he described above with respect to his rejection of claims 9 and 10.

IX. ARGUMENT

A. The Section 112, Second Paragraph Rejection of Claims 1-3 and 5-10

Concurrent with the Notice of Appeal in this case, Appellants filed an amendment to claim 1 to address the Examiner's indefiniteness rejection. Appellants respectfully submit that the amendment to claim 1 presented with the Notice of Appeal (and repeated in the amendment attached to this Appeal Brief) properly addresses the Examiner's concerns. Accordingly, Appellants respectfully request withdrawal of the 35 U.S.C. §112 rejection of claims 1-3 and 5-10.

B. The Section 103 Rejections of Claims 1-3 and 5-10

Appellants respectfully submit that Ozawa in view of the Examiner's remarks does not render claims 1-3 and 5-10 obvious for at least the following reasons.

1. The *Prima Facie* Case of Obviousness

The legal concept of *prima facie* obviousness is a procedural tool of examination which applies broadly to all arts. A prima facie case of obviousness is one that will stand unless rebutted by evidence. It is the burden of the examiner to establish a prima facie case of obviousness when rejecting claims under 35 U.S.C. §103. In re Piasecki, 754 F.2D 1468, 223 USPQ 758 (Fed. Cir. 1985); MPEP §2142.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Next, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000).

2. The combination of Ozawa and the Examiner's Remarks does not teach all the elements recited in claims 1-3 and 5-10

Appellants respectfully submit that Ozawa in view of the Examiner's remarks does not teach all the elements of claim 1 because neither Ozawa nor the Examiner's

remarks teach either the element of "at least one metal layer" or the element of "at least one zag conductor . . . so as to interconnect components on said integrated circuit" as recited in amended claim 1. In one embodiment, Ozawa describes a semiconductor device comprising a substrate and two semiconductor elements each attached to different surfaces of the substrate. The substrate further comprises built in wires which enable the electrodes of one semiconductor element to be connected to electrodes of the other semiconductor element. Col. 2, lines 21-43. The semiconductor device described in Ozawa is intended to solve problems associated with connecting electrodes between two semiconductor elements when the electrode layouts of the semiconductor elements are different (i.e., the electrodes of one semiconductor element and the electrodes of the other semiconductor element (when the semiconductor elements are attached to opposite surfaces of the substrate) cannot be connected through an imaginary line perpendicular to the surface of the substrate). Prior to Ozawa, large loops of wires would be required to connect the electrodes of semiconductor elements attached to a substrate when the electrode layouts for the semiconductor elements were different. Col. 6, lines 50-64.

In the Final Office Action, the Examiner suggests that the substrate 33 described in Ozawa teaches the at least one metal layer element recited in claim 1. However, nothing in Ozawa describes the substrate 33 as being comprised of metal. In fact, Ozawa states that the substrate may be made of "polyimide" or "glass epoxy" as the basic

material. Col. 5, lines 38-42. Thus, Ozawa does not teach a metal layer as recited in amended claim 1.

In addition to failing to teach the "at least one metal layer" element of claim 1, nothing in Ozawa teaches utilizing a zag conductor to interconnect components of an integrated circuit as recited in amended claim 1. As mentioned above, Ozawa teaches a method for interconnecting electrodes of semiconductor devices. As defined in Appellants' specification, components of an integrated circuit may include electronic components (such as transistors, resistors, and diodes) and circuit components (such as gates, cells, arithmetic units, controllers, and decoders). Nothing in Ozawa teaches interconnecting components as recited in amended claim 1.

In addition to failing to teach both the "at least one metal layer" element and the interconnection of components element, Ozawa also fails to teach the element of amended claim 1 which recites that the first contiguous region comprises an area of at least 100 square microns. The Examiner admits to this deficiency in the Final Office Action. To make up for this Ozawa deficiency, the Examiner cites In re Rose, 105 USPQ 237 (CCPA 1955), and asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify what he asserts is a first contiguous region of Ozawa to have any area greater than, less than, or equal to 100 square microns. MPEP §2144 states that if the facts in a prior legal decision are sufficiently similar to those in an application under examination, the examiner may use the rationale used by the

court. However, the facts of In re Rose are not at all similar to the present application. In In re Rose, the claims were directed to a lumber package. The claim language recited that the weight of lumber packages covered by the scope of that claim were lumber packages "of appreciable size and weight requiring handling by a lift truck". Id. The court held this claim to be unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art. Id. In addition to the fact that the subject matter of In re Rose (a lumber package) is nonanalogous to the art area of the present application (conductors within integrated circuits), the claim language was very vague: of appreciable size and weight requiring handling by a lift truck. In the present case, the claim language in question is very specific: an area of a metal layer of at least 100 square microns. Thus, Appellants respectfully submit that the facts of In re Rose are not sufficiently similar to the facts of the present application as required by MPEP §2144 and that In re Rose has not been properly cited by the Examiner to support the 35 U.S.C. §103 rejection of claims 1-3 and 5-10.

In addition to respectfully submitting that the Examiner has improperly cited In re Rose to make up for the deficiency that Ozawa does not teach the 100 square micron element of claim 1, Appellants respectfully disagree with the Examiner's assertion that this same deficiency of Ozawa may be made up because a change in size in the context of the 100 square micron element recited in claim 1 would be well known to one of ordinary

skill in the art at the time the present invention was made. Thus, in accordance with MPEP §2144.03, the Examiner is requested to provide a reference or references supporting all of the features the Examiner believes are "well known". If the rejection is based on facts within the personal knowledge of the Examiner, the Examiner is requested to support the rejection with an affidavit setting forth the facts upon which the Examiner's rejection is based. See 37 C.F.R. 1.104(d)(2). Appellants should be given an opportunity to address the new reference(s) or affidavit.

In view of the above, Appellants respectfully submit that the Ozawa in view of the Examiner's remarks does not render obvious the subject matter of claim 1 because this combination does not teach each element of claim 1. Withdrawal of this rejection of claim 1 under 35 U.S.C. §103(a) is, therefore, requested.

As for claims 2, 3, and 5-10, each of these claims is dependent either directly or indirectly from independent claim 1. Accordingly, the arguments made above apply equally to these claims. Withdrawal of the rejection of claims 2, 3, and 5-10 under 35 U.S.C. §103 is therefore requested.

C. The Section 103 Rejections of Claims 11-13 and 15-20

Appellants respectfully submit that Rostoker in view of the Examiner's remarks or in view of Ozawa does not render claims 11-13 and 15-20 obvious for at least the following reasons.

Appellants respectfully submit that Rostoker in view of the Examiner's remarks or in view of Ozawa does not teach all the elements of claim 11 because neither Rostoker, the Examiner's remarks, nor Ozawa teach "at least one zag conductor coupled to a conductor deposed in a first diagonal direction, . . . said zag conductor being on a same metal layer as said conductor deposed in the first diagonal direction." as recited in claim 11. Rostoker teaches an architecture which provides electrical conductors for interconnection. Col. 6, lines 31-33. In accordance with the preferred embodiment, three separate metal layers comprise conductors. The conductors on each metal layer extend in three different directions that are angularly displaced from each other by 60 degrees. Thus, for example, the conductors of metal layer 1 are displaced 60 degrees in direction from the conductors of metal layer 2; the conductors of metal layer 2 are displaced 60 degrees in direction from the conductors of metal layer 3. Col. 6, lines 31-48. Deposing the conductors as described above provides more than the traditional two directions of interconnect routing provided by the prior art. Col. 4, lines 54-60. According to Rostoker, this architecture is advantageous because these additional routing directions reduce the total wirelength interconnect congestion of integrated circuits. Col. 6, lines 48-54. However, unlike the present invention, nothing in Rostoker teaches coupling conductors to each other wherein the coupled conductors are on the same metal layer. In fact, unlike the present invention as recited in claim 1, Rostoker teaches away from

coupling conductors on the same metal layer wherein the conductors are deposed in different directions:

> Conductors that extend in the three directions can be formed in three different layers, or alternatively the conductors that extend in two or three of the directions can be formed in a single layer as long as they do not cross. Col. 7, lines 60-63.

See also Rostoker at Col. 17, lines 1-6. Unlike the coupling recited in claim 11, Rostoker teaches that the conductors within a same metal layer should not cross. When the prior art teaches away from the present invention, a per se demonstration that there is a lack of prima facie obviousness arises. In re Dow Chemical Co., 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1988).

In addition to failing to teach coupling of conductors within a single metal layer as recited in claim 11, the Examiner admits that Rostoker does not explicitly teach zag conductors. The Examiner suggests that Rostoker implicitly teaches zag conductors at Col. 6, lines 7-15, Col. 6, lines 1-20, and Col. 7, line 60-Col. 8, line 4. Appellants respectfully submit that these sections of Rostoker do not teach a zag conductor coupled to a conductor deposed in a diagonal direction as recited in claim 11. Appellants respectfully disagree with the Examiner's conclusion that it would have been obvious to one of ordinary skill in the art at the time the invention was made that Rostoker teaches zag conductors coupled to conductors deposed in a diagonal direction. Thus, in accordance with MPEP §2144.03, the Examiner is requested to provide a reference or

references supporting all of the features the Examiner believes are "well known". If the rejection is based on facts within the personal knowledge of the Examiner, the Examiner is requested to support the rejection with an affidavit setting forth the facts upon which the Examiner's rejection is based. See 37 C.F.R. 1.104(d)(2). Appellants should be given an opportunity to address the new reference(s) or affidavit.

Appellants respectfully submit that there is no motivation to combine the teachings of Rostoker and Ozawa. The mere fact that references can be combined or modified does not render the resultant combination obvious, unless the prior art also suggests the desirability of the combination. In re Kotzab, supra. It is improper to use the inventor's disclosure as a road map for selecting and combining prior art disclosures. Grain Processing Corp. v. American Maize-Products Corp., 840 F.2d 902, 907 (Fed. Cir. 1988). Absent such a showing in the prior art, the Examiner has impermissibly used "hindsight" by using the Appellants' teaching as a blueprint to hunt through the prior art for the claimed elements and combine them as claimed. In re Zuko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997). Appellants respectfully submit that the Examiner is relying on an improper hindsight reconstruction, which cannot be used for rejecting the claims of the above-identified application. Nothing in Rostoker or Ozawa teach or suggest combining the teachings of their respective disclosures.

Because Rostoker does not teach coupling a zag conductor to a conductor deposed in a diagonal direction wherein both conductors are on the same metal layer, because the Examiner admits that Rostoker fails to teach the zag conductor element, and because there is no motivation to combine Rostoker and Ozawa, the combination of Rostoker in view of the Examiner's remarks or in view of Ozawa does not render claim11 obvious under 35 U.S.C. §103(a). Accordingly, Appellants respectfully request withdrawal of the rejection of claim 11.

As for claims 12, 13, and 15-20, each of these claims is dependent either directly or indirectly from independent claim 11. Accordingly, the arguments made above apply equally to these claims. Withdrawal of the rejection of claims 12, 13, and 15-20 under 35 U.S.C. §103 is therefore requested.

X. CONCLUSION.

For the foregoing reasons, Appellants believe that the Examiner's rejections of claims 1-3, 5-13, and 15-20 were erroneous, and reversal of his decisions is respectfully requested.

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APPENDIX

The following claims are the subject of this Appeal.

1. An integrated circuit comprising:

at least one metal layer comprising a plurality of regions, wherein a first contiguous region comprises an area of said metal layer of at least 100 square microns and comprises a plurality of conductors to interconnect components on said integrated circuit, said conductors comprising a plurality of preferred diagonal direction conductors and at least one zag conductor, and wherein a second contiguous region comprises a plurality of conductors such that at least fifty (50) percent of said conductors of the second contiguous region are arranged in a preferred direction other than said preferred diagonal direction;

said preferred diagonal direction conductors comprising at least fifty (50) percent of said conductors in said first region and being deposed in a preferred diagonal direction that forms a Euclidean angle relative to the boundaries of the integrated circuit, and

said at least one zag conductor being deposed in a Manhattan direction and being coupled to one of said preferred diagonal direction conductors so as to interconnect components on said integrated circuit using at least one zag conductor and at least one preferred diagonal direction conductor.

2. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises plus 45 degrees relative to the boundaries of said integrated circuit.

3. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises minus 45 degrees relative to the boundaries of said integrated circuit.

Claim 4 (cancelled)

5. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises plus 60 degrees relative to the boundaries of said integrated circuit.

6. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises minus 60 degrees relative to the boundaries of said integrated circuit.

7. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises plus 30 degrees relative to the boundaries of said integrated circuit.

8. The integrated circuit of claim 1, wherein said preferred diagonal direction comprises minus 30 degrees relative to the boundaries of said integrated circuit.

9. The integrated circuit of claim 1, wherein said Manhattan direction of said at least one zag comprises a horizontal direction relative to the boundaries of said integrated circuit.

10. The integrated circuit of claim 1, wherein said Manhattan direction of said at least one zag comprises a vertical direction relative to the boundaries of said integrated circuit.

11. An integrated circuit comprising:

a plurality of metal layers with each metal layer comprising a plurality of conductors to interconnect components on the integrated circuit, at least fifty (50) percent of said conductors on a first metal layer being deposed in a first preferred diagonal direction, wherein said first preferred diagonal direction defines a direction that forms a Euclidean angle relative to the boundaries of the integrated circuit, for at least fifty percent of conductors on said first metal layer;

at least fifty (50) percent of said conductors on a second metal layer arranged in a second preferred diagonal direction, wherein said second preferred diagonal direction defines a direction, different than said first preferred diagonal direction, that forms a Euclidean angle relative to the boundaries of the integrated circuit; and

at least one zag conductor, coupled to a conductor deposed in a first diagonal direction, said zag conductor being deposed in a Manhattan direction so as to interconnect components on said integrated circuit using at least one zag conductor and at least one conductor arranged in said first preferred diagonal direction, said zag conductor being on a same metal layer as said conductor deposed in the first diagonal direction.

12. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises plus 45 degrees and said second preferred diagonal direction comprises minus 45 degrees relative to the boundaries of said integrated circuit.

13. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises minus 45 degrees and said second preferred diagonal direction comprises plus 45 degrees relative to the boundaries of said integrated circuit.

Claim 14 (cancelled)

15. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises plus 60 degrees and said second preferred diagonal direction comprises minus 60 degrees relative to the boundaries of said integrated circuit.

16. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises minus 60 degrees and said second preferred diagonal direction comprises plus 60 degrees relative to the boundaries of said integrated circuit.

17. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises plus 30 degrees and said second preferred diagonal direction comprises minus 30 degrees relative to the boundaries of said integrated circuit.

18. The integrated circuit of claim 11, wherein said first preferred diagonal direction comprises minus 30 degrees and said second preferred diagonal direction comprises plus 30 degrees relative to the boundaries of said integrated circuit.

19. The integrated circuit of claim 11, wherein said Manhattan direction of said at least one zag conductor comprises a horizontal direction relative to the boundaries of said integrated circuit.

20. The integrated circuit of claim 11, wherein said Manhattan direction of said at least one zag conductor comprises a vertical direction relative to the boundaries of said integrated circuit.

Claims 21-47 (cancelled)